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Substitute for form 1449A/PTO <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  <i>(use as many sheets as necessary)</i>				<b>Complete if Known</b>	
				Application Number	Not Yet Assigned
				Filing Date	September 26, 2003
				First Named Inventor	Warren M. Farnworth
				Group Art Unit	Unknown
				Examiner Name	Unknown
Sheet	1	of	1	Attorney Docket Number	2269-3996.2US (99-0254.02/US)

[illegible][illegible]

Examiner Signature	/Leo B. Tentoni/	Date Considered	09/28/2006
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PTO/SB/08A (10-01)

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**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**

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Sheet 1 of 6

Complete if Known

Application Number	10/672,098
Filing Date	September 26, 2003
First Named Inventor	Warren M. Farnworth
Group Art Unit	Unknown
Examiner Name	Unknown
Attorney Docket Number	3996.2US (99-0254.02/US)

**U.S. PATENT DOCUMENTS**

Examiner Initials *	Cite No. <sup>1</sup>	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code <sup>2</sup> (if known)			
LBT		US-6,251,488	08/26/01	Miller et al.	
		US- 6,259,982	07/10/01	Gothait	
		US- 6,268,584	07/31/01	Keicher et al.	
		US- 6,326,698	12/04/01	Akram	
		US- 6,337,122	01/08/02	Grigg et al.	
		US- 6,391,251	05/21/02	Keicher et al.	
		US- 6,432,752	08/13/02	Farnworth	
		US-6,482,576	11/19/02	Farnworth et al.	
		US- 6,489,007	12/03/02	Grigg et al.	
		US- 6,508,871	01/14/03	Grigg	
		US- 6,514,798	02/04/03	Farnworth	
		US- 6,524,346	02/25/03	Farnworth	
		US- 6,525,408	02/25/03	Akram et al.	
		US- 6,544,465	04/08/03	Farnworth et al.	
		US- 6,544,821	04/08/03	Akram	
		US- 6,544,902	04/08/03	Farnworth	
		US- 6,548,897	04/15/03	Grigg	
		US- 6,562,278	05/13/03	Farnworth et al.	
		US- 6,569,753	05/27/03	Akram et al.	
		US- 6,585,927	07/01/03	Grigg et al.	
		US- 6,593,171	07/15/03	Farnworth	
		US-6,607,689	08/19/03	Farnworth	
LBT		US-6,635,333	10/21/03	Grigg et al.	

**FOREIGN PATENT DOCUMENTS**

Examiner Initials *	Cite No. <sup>1</sup>	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>6</sup>
		Country Code <sup>3</sup> - Number <sup>4</sup> - Kind Code <sup>5</sup> (if known)				

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/Leo B. Tentoni/

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Sheet 2 of 6

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First Named Inventor	Warren M. Farnworth
Group Art Unit	Unknown
Examiner Name	Unknown
Attorney Docket Number	3996 21JS (99-0254 02/1JS)

**OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS**

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LBT		U.S. Patent Application Publication 2002/0066966 A1 to Farnworth, dated June 6, 2002	
		U.S. Patent Application Publication 2002/0098623 A1 to Akram, dated July 25, 2002	
		U.S. Patent Application Publication 2002/0105074 A1 to Akram et al., dated August 8, 2002	
		U.S. Patent Application Publication 2002/0171177 A1 to Krichman et al., dated November 21, 2002	
		U.S. Patent Application Publication 2002/0182782 A1 to Farnworth, dated December 5, 2002	
		U.S. Patent Application Publication 2002/0195748 A1 to Farnworth, dated December 26, 2002	
		U.S. Patent Application Publication 2003/0003179 A1 to Farnworth et al., dated January 2, 2003	
		U.S. Patent Application Publication 2003/0003180 A1 to Farnworth et al., dated January 2, 2003	
		U.S. Patent Application Publication 2003/0003380 A1 to Farnworth et al., dated January 2, 2003	
		U.S. Patent Application Publication 2003/0003405 A1 to Farnworth et al., dated January 2, 2003	
↓		U.S. Patent Application Publication 2003/0068584 A1 to Farnworth et al., dated April 10, 2003	
LBT		U.S. Patent Application Publication 2003/0072926 A1 to Grigg et al., dated April 17, 2003	

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LBT		U.S. Patent Application Publication 2003/0077418 A1 to Grigg et al., dated April 24, 2003	
		U.S. Patent Application Publication 2003/0089999 A1 to Akram, dated May 15, 2003	
		U.S. Patent Application Publication 2003/0092220 A1 to Akram, dated May 15, 2003	
		U.S. Patent Application Publication 2003/0093173 A1 to Farnworth et al., dated May 15, 2003	
		U.S. Patent Application Publication 2003/0098499 A1 to Akram et al., dated May 29, 2003	
		U.S. Patent Application Publication 2003/0102566 A1 to Farnworth, dated June 5, 2003	
		U.S. Patent Application Publication 2003/0129787 A1 to Farnworth, dated July 10, 2003	
		U.S. Patent Application Publication 2003/0139030 A1 to Grigg, dated July 24, 2003	
		U.S. Patent Application Publication 2003/0151167 A1 to Krichman et al., dated August 14, 2003	
		U.S. Patent Application Publication 2003/0155693 A1 to Farnworth et al., dated August 21, 2003	
↓			
LBT		U.S. Patent Application Publication 2003/0173665 A1 to Grigg, dated September 18, 2003	

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LBT		U.S. Patent Application Publication 2003/0176016 A1 to Grigg, dated September 18, 2003	
		U.S. Patent Application Publication 2003/0193092 A1 to Tan et al., dated October 16, 2003	
		U.S. Patent Application Publication 2003/0201531 A1 to Farnworth et al., dated October 30, 2003	
		U.S. Patent Application Publication 2003/0203158 A1 to Farnworth et al., dated October 30, 2003	
		U.S. Patent Application Publication 2003/0203612 A1 to Akram et al., dated October 30, 2003	
		U.S. Patent Application Publication 2003/0205849 A1 to Farnworth, dated November 6, 2003	
		MILLER et al., "Maskless Mesoscale Materials Deposition", Deposition Technology, September 2001, pages 20-22	
		MILLER, "New Laser-Directed Deposition Technology", Microelectronic Fabrication, August 2001, page 16	
✓		Webpage, Objet Prototyping the Future, "Objet FullCure700 Series", 1 page	
LBT		Webpage, Objet Prototyping the Future, "How it Works", 2 pages	
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LBT		U.S. Patent Application No. 09/589,841, filed June 8, 2000, entitled "Stereolithographic Methods for Forming a Protective Layer on a Semiconductor Device Substrate and Substrates Including Protective Layers So Formed", inventor Farnworth et al.	
		U.S. Patent Application No. 09/590,646, filed June 8, 2000, entitled "Reinforced, Self-Aligning Conductive Structures for Semiconductor Device Components and Methods for Fabricating Same", inventor Williams et al.	
		U.S. Patent Application No. 09/651,930, filed August 31, 2000, entitled "Semiconductor Device Including Leads in Communication with Contact Pads Thereof and a Stereolithographically Fabricated Package Substantially Encapsulating the Leads and Methods for Fabricating the Same", inventor Salman Akram	
		U.S. Patent Application No. 10/191,424, filed July 8, 2002, entitled "Semiconductor Devices with Permanent Polymer Stencil and Method for Manufacturing the Same", inventor Farnworth et al.	
		U.S. Patent Application No. 10/201,208, filed July 22, 2002, entitled "Thick Solder Mask for Confining Encapsulant Material Over Selected Locations of a Substrate, Assemblies Including the Solder Mask, and Methods", inventor Grigg et al.	
		U.S. Patent Application 10/370,755, filed February 20, 2003, entitled "Chip Scale Package Structures and Method of Forming Conductive Bumps Thereon", inventor Warren M. Farnworth	
		U.S. Patent Application No. 10/608,749, filed June 26, 2003, entitled "Methods for Labeling Semiconductor Device Components", inventor Grigg et al.	
V LBT		U.S. Patent Application No. 10/619,918, filed July 15, 2003, entitled "Stereolithographic Methods for Fabricating Hermetic Semiconductor Device Packages and Semiconductor Devices Including Stereolithographically Fabricated Hermetic Packages", inventor Warren M. Farnworth	
		U.S. Patent Application No. 10/642,908, filed August 18, 2003, entitled "Solder Masks for Use on Carrier Substrates, Carrier Substrates and Semiconductor Device Assemblies Including Such Solder Masks, and Methods", inventor Tan et al.	
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Sheet	6	of	6		

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LBT		U.S. Patent Application No. 10/663,402, filed September 16, 2003, entitled "Processes for Facilitating Removal of Stereolithographically Fabricated Objects from Platens of Stereolithographic Fabrication Equipment, Object Release Elements for Effecting Such Processes, Systems and Fabrication Processes Employing the Object Release Elements, and Objects Which Have Been Fabricated Using the Object Release Elements", inventor Farnworth et al.			
LBT		U.S. Patent Application No. 10/688,354, filed October 17, 2003, entitled "Thick Solder Mask for Confining Encapsulant Material Over Selected Locations of a Substrate and Assemblies Including the Solder Mask", inventor Grigg et al.			
LBT		U.S. Patent Application No. 10/690,417, filed October 20, 2003, entitled "Methods of Coating and Singulating Wafers and Chip-Scale Packages Formed Therefrom", inventor Farnworth et al.			
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Sheet

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**First Named Inventor**

Warren M. Farnworth

### Group Art Unit

Unknown

**Examiner Name**

## Unknown

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**Examiner  
Signature**

/Leo B. Tentoni/

Date Considered

09/28/2006

**\*EXAMINER:** Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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## INFORMATION DISCLOSURE STATEMENT BY APPLICANT

*(use as many sheets as necessary)*

Sheet

1

of

1

Application Number

**Complete if Known**

10/672.098

Filing Date

**September 26, 2003**

**First Named Inventor**

Warren M. Farnworth

**Group Art Unit**

1722

Examiner Name

**Unknown**

Attorney Docket Number

2269-3996.2US (99-0254.02/US)

## U.S. PATENT DOCUMENTS

[illegible]

## FOREIGN PATENT DOCUMENTS

[illegible]

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